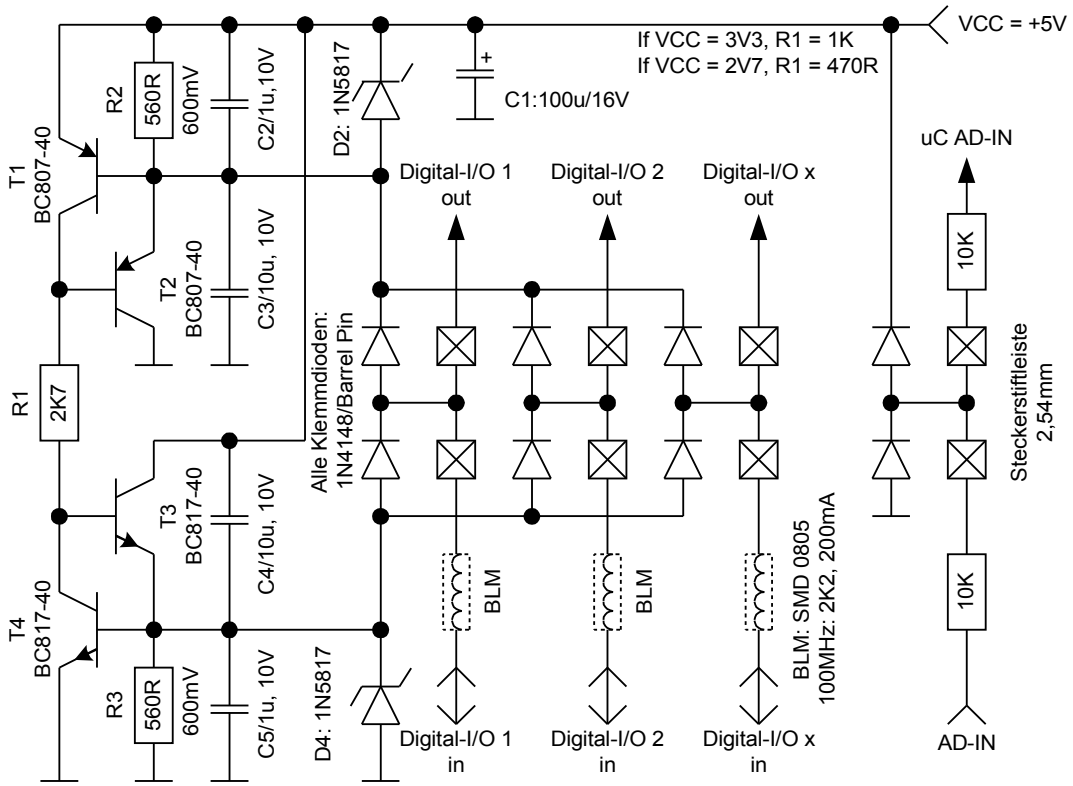
Externe, aktive FPGA- & uController I/O-Port ESD-Schutzschaltung:
Falls keine ESD geschützten I/O Port ICs verwendet werden können, bildet diese Art Schaltung einen alternativen ESD Schutz.
Es werden eine Vielzahl von ESD-Klemmarrays angeboten wie z.B. SEMTECH, bitte Datenblatt ansehen.
Eine präzise Überspannungs- & Unterspannungsklemmung bewirkt allerdings keiner.

Aktive ESD-Klemmschaltung, VCC = 5V

Überspannungspulse > 5V:
An T2-E steht eine geregelte Spannung von -600mV gegenüber VCC an.
Durch die Serienbeschaltung von C2 & C3 wird die Strecke VCC und GND gegenüber Spannungsspitzen niederohmig.
Eine an Digital-I/O-1 anliegende Eingangsspannungen > +5V wird durch die bereits bei +4V4 leitenden Diode nach GND-Potenzial abgeleitet.

Unterspannungspulse < GND:
An T3-E steht eine geregelte Spannung von +600mV gegenüber GND an.
Durch die Serienbeschaltung von C4 & C5 wird die Strecke VCC und GND gegenüber Spannungsspitzen niederohmig.
Eingangsspannungen < GND werden durch die bereits bei +600mV voll leitende Diode nach GND-Potenzial abgeleitet.

Begrenzung von Spannungsspitzen durch BLMs:
BLMs werden bei 100 MHz im ps-Bereich hochohmig und können so schnelle Eingangsimpulse unterdrücken.



ATMEGA32U4, ATMEGA-8 I/O-Port Spec.

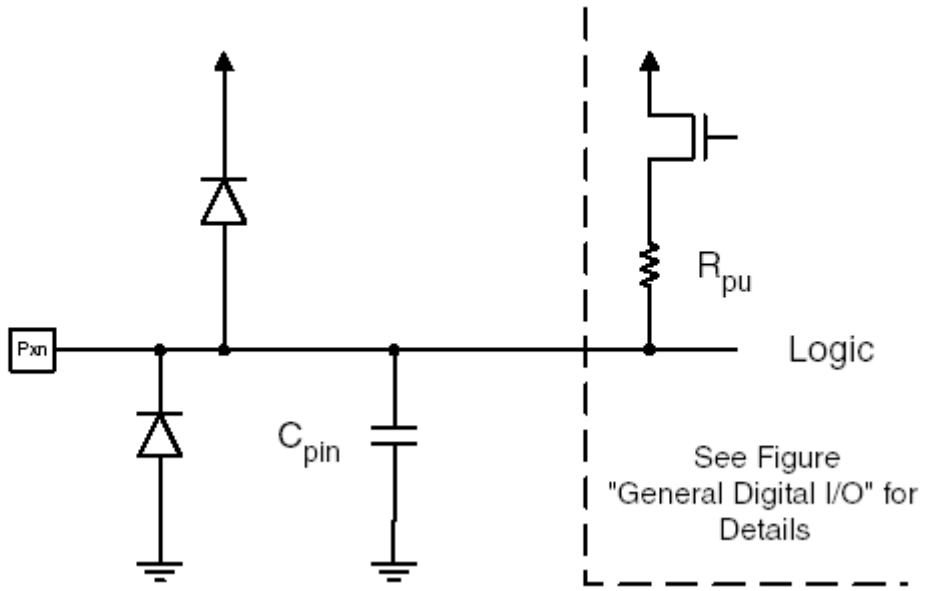
Für XILINXS FPGA's konnte ich leider keine Beschreibung der I/O-Port Schaltung finden, wird aber so wie von ATMEL ausgelegt sein.

28.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

ATMEGA32U4, ATMEGA-8 I/O-Port Protection:

Figure 13-1. I/O Pin Equivalent Schematic



Die beiden bipolaren Schutzdioden benötigen etwa 6nS um voll leitfähig zu werden. C-pin etwa 6nF.
ESD-Spannung im ps Bereich schädigen die CMOS-Struktur lange bevor die bipolaren Schutzdioden leitfähig werden!

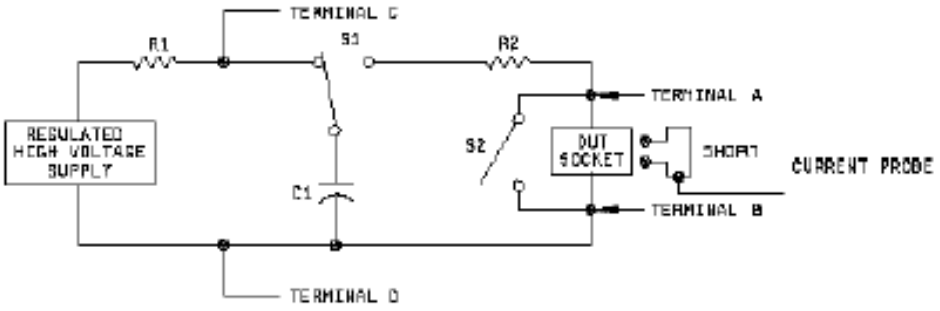
Die Gefahr einer möglichen, statische ESD-Aufladung & Entladung sollte man im Umgang mit FPGA's & uControllern im power up- & power down Modus immer Betracht ziehen!
Human Body ESD model: discharging high voltage from the finger tips of a standing person that touches an IC:
Mit synthetischer Kleidung: Kunststoffsohlen auf Kunstfaserteppich, die statische Spannung kann locker > 8kV ereichen !

Human Body Model (HBM) and Machine Model (MM)

The Human Body Model is the oldest and best-known ESD model. The HBM dates back to the 1800s. This model first gained acceptance in the semiconductor industry in the late 1960s as a method for simulating failures of Junction Field Effect Transistors (JFETs) used in the Flight Control Computer for the United States Titan III Space Program. The model consists of a simple series RC circuit with the values of R and C selected to simulate the discharge from the fingertip of a standing person that touches an IC. Although the HBM was used extensively during the 1970s, lack of consensus on a standard for test systems (in particular, what values of R and C to use) resulted in poor correlation between HBM thresholds measured using different ESD test systems.

Correlation between testers greatly improved after MIL-STD-883 Method 3015 *Electrostatic Discharge Sensitivity Classification* was released in 1979[1]. This HBM test method specifies an RC network of R_2 = 1500Ω and C_1 = 100pF, as shown in Figure 1. Real-world RC values vary considerably from person-to-person and are a function of many variables, including the person's clothing/shoes, position, and surroundings. Consequently, the 1500Ω, 100pF model should be considered more of a benchmark than a true model for discharges from people's fingers. Per Figure 1, capacitor C1 is charged via a high voltage generator in series with a charge resistor R1. When high voltage relay S1 is thrown, the voltage V_{ESD} on C1 is discharged as current I_{ESD} through the series combination of discharge resistor R2 and the Device Under Test (DUT). The peak value of I_{ESD} is given by:

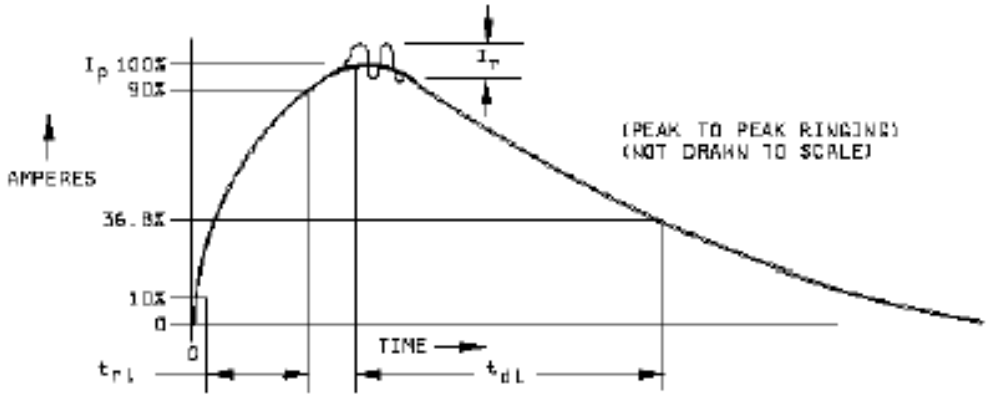
$$(1) \qquad I_P = V_{ESD}/(R_2 + R_{DUT}).$$



R1 = 10^6 ohms to 10^7 ohms
C1 = 100 picoFarads ±10 percent (Insulation resistance 10^{12} ohms minimum)
R2 = 1,500 ohms ±1 percent
S1 = High voltage relay (Bounceless, mercury wetted, or equivalent)
S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

Figure 1: HBM ESD Test Circuit
(Excerpted from MIL-STD-883 Method 3015.7)

Sollte man sich im Umgang mit FPGA's & uControllern im power up- & power down Modus vor Augen halten.



The current pulse shall have the following characteristics:

Tri (rise time) ----------	Less than 10 nanoseconds.
Tdi (delay time) ----------	150 ±20 nanoseconds.
Ip (peak current) ----------	Within ±10 percent of the Ip value shown in Table 1 for the voltage step selected.
Ir (ringing) ----------	The decay shall be smooth, with ringing, break points, double time constants or discontinuities less than 15 percent Ip maximum, but not observable 100 nanoseconds after start of the pulse.

Figure 2: HBM ESD Short-Circuit Current Waveform (Excerpted from MIL-STD-883 Method 3015.7)

The HBM ESD test circuit in Figure 1 essentially acts as an ideal current source that injects current into the DUT. Figure 2 shows the ESD current, I_{ESD}, vs. time when the DUT is a short-circuit ($R_{DUT} = 0\Omega$). This HBM ESD waveform has a characteristic double exponential shape, with a rise time typically in the 6-8ns range and a fall-time of $\tau = (R_2)(C_1) = (1500\Omega)(100pF) = 150ns$.

Table 1 shows the peak HBM ESD current, I_P, into a short-circuit ($R_{DUT} = 0\Omega$) for the typical minimum set of stress voltages used to classify the HBM ESD robustness of ADI products. Substituting $R_{DUT} = 0\Omega$ into equation (1), $I_{P(0\Omega)} = V_{ESD}/R_2$, or $I_{P(0\Omega)} = V_{ESD}/1500\Omega$. Thus, for a 1000V HBM event into a short-circuit, $I_{P(0\Omega)} = 1000V/1500\Omega$ or 0.67 Amp.

Table 1: ADI HBM ESDS Testing Stress Levels and Associated Classifications

Stress Voltage	Peak Current, I_P (±10%)	Sample Size	Corresponding HBM ESDS Classification for any electrical failures at this stress voltage
+500V	+0.33A	3	Class 1
±1000V	±0.67A	3	Class 1
±1500V	±1.00A	3	Class 1
±2000V	±1.33A	3	Class 1
±2500V	±1.67A	3	Class 2
±3000V	±2.00A	3	Class 2
±3500V	±2.33A	3	Class 2
±4000V*	±2.67A	3	Class 2

* If all samples pass following stress testing through ±4000V, the HBM ESDS classification is Class 3.