

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	CPU	Notes
Endpoint 0-7 Data Buffers												Access	CPU Access Codes:
7B40	OUT7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	RW = Read or Write,
7B80	IN7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	R, r = read-only,
7BC0	OUT6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	W, w = write-only
7C00	IN6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	b = both (Read & Write)
7C40	OUT5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7C80	IN5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7CC0	OUT4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7D00	IN4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7D40	OUT3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7D80	IN3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7DC0	OUT2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7E00	IN2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7E40	OUT1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7E80	IN1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7EC0	OUT0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7F00	IN0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7F40-7F5F (reserved)													
Isochronous Data													
7F60	OUT8DATA	Endpoint 8 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F61	OUT9DATA	Endpoint 9 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F62	OUT10DATA	Endpoint 10 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F63	OUT11DATA	Endpoint 11 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F64	OUT12DATA	Endpoint 12 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	W	

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	CPU	Notes
	Isochronous Byte Counts											Access	
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8	xxxxxxxx	R	
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
	7F80-7F91 (reserved)												
	CPU Registers												
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	0	0	CLK24OE	8051RES	()0011	rrrrrrbr	rv[3..0] = chip rev
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out	00000000	RW	0=port, 1=alt function
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2	00000000	RW	0=port, 1=alt function
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0	00000000	RW	0=port, 1=alt function
	Input-Output Port Registers												
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0	00000000	RW	
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0	00000000	RW	
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0	00000000	RW	
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	xxxxxxxx	R	
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	xxxxxxxx	R	
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	xxxxxxxx	R	
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0	00000000	RW	0=off, 1=drive
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0	00000000	RW	0=off, 1=drive
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0	00000000	RW	0=off, 1=drive
7F9F		(reserved)											
	Isochronous Control/Status Registers												
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15ERR	ISO14ERR	ISO13ERR	ISO12ERR	ISO11ERR	ISO10ERR	ISO9ERR	ISO8ERR	xxxxxxxx	R	
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	MBZ	MBZ	ISODISAB	0000x000	rrrrrrbbb	"MBZ" = Must Be Zero
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	xxxxxxxx	R	
7FA3		(reserved)											
7FA4		(reserved)											
	I²C Registers												
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr	
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
7FA7		(reserved)											

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	CPU	Notes
	Interrupts											Access	
7FA8	IV _{EC}	Interrupt Vector	0	IV ₄	IV ₃	IV ₂	IV ₁	IV ₀	0	0	00000000	R	
7FA9	IN _{07IRQ}	EPIN Interrupt Request	IN _{7IR}	IN _{6IR}	IN _{5IR}	IN _{4IR}	IN _{3IR}	IN _{2IR}	IN _{1IR}	IN _{0IR}	00000000	RW	1=request
7FAA	OUT _{07IRQ}	EPOUT Interrupt Request	OUT _{7IR}	OUT _{6IR}	OUT _{5IR}	OUT _{4IR}	OUT _{3IR}	OUT _{2IR}	OUT _{1IR}	OUT _{0IR}	xxxxxxxx	RW	1=request
7FAB	US _{BIRQ}	USB Interrupt Request	*	*	*	URES _{IR}	SUS _{PIR}	SUTOK _{IR}	SOF _{IR}	SUDAV _{IR}	00000000	RW	1=request
7FAC	IN _{07IEN}	EP0-7IN Int Enables	IN _{7IEN}	IN _{6IEN}	IN _{5IEN}	IN _{4IEN}	IN _{3IEN}	IN _{2IEN}	IN _{1IEN}	IN _{0IEN}	00000000	RW	1=enabled
7FAD	OUT _{07IEN}	EP0-7OUT Int Enables	OUT _{7IEN}	OUT _{6IEN}	OUT _{5IEN}	OUT _{4IEN}	OUT _{3IEN}	OUT _{2IEN}	OUT _{1IEN}	OUT _{0IEN}	00000000	RW	1=enabled
7FAE	US _{BIEN}	USB Int Enables	*	*	*	URES _{IE}	SUS _{PIE}	SUTOK _{IE}	SOF _{IE}	SUDAV _{IE}	00000000	RW	1=enabled
7FAF	US _{BB_{AV}}	Breakpoint & Autovector	*	*	*	*	BREA _K	BPPUL _{SE}	BPEN	AVEN	xxxxxx00	RW	1=enabled
7FB0		(reserved)											
7FB1		(reserved)											
7FB2	BPADDR _H	Breakpoint Address H	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	00000000	RW	
7FB3	BPADDR _L	Breakpoint Address L	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	00000000	RW	
	Bulk Endpoints 0-7												
7FB4	EP _{0CS}	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP ₀ STALL	00001000	rrrrrrbb	For EP ₀ IN and EP ₀ OUT
7FB5	IN _{0BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	* this bits are random
7FB6	IN _{1CS}	Control & Status	*	*	*	*	*	*	in ₁ bsy	in ₁ stl	00000000	rrrrrrrb	at power-on. Once
7FB7	IN _{1BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	operational, these bits
7FB8	IN _{2CS}	Control & Status	*	*	*	*	*	*	in ₂ bsy	in ₂ stl	00000000	rrrrrrrb	read as zeros.
7FB9	IN _{2BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FBA	IN _{3CS}	Control & Status	*	*	*	*	*	*	in ₃ bsy	in ₃ stl	00000000	rrrrrrrb	
7FBB	IN _{3BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FBC	IN _{4CS}	Control & Status	*	*	*	*	*	*	in ₄ bsy	in ₄ stl	00000000	rrrrrrrb	
7FBD	IN _{4BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FBE	IN _{5CS}	Control & Status	*	*	*	*	*	*	in ₅ bsy	in ₅ stl	00000000	rrrrrrrb	
7FBF	IN _{5BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FC0	IN _{6CS}	Control & Status	*	*	*	*	*	*	in ₆ bsy	in ₆ stl	00000000	rrrrrrrb	
7FC1	IN _{6BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FC2	IN _{7CS}	Control & Status	*	*	*	*	*	*	in ₇ bsy	in ₇ stl	00000000	rrrrrrrb	
7FC3	IN _{7BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FC4		(reserved)											
7FC5	OUT _{0BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FC6	OUT _{1CS}	Control & Status	*	*	*	*	*	*	out ₁ bsy	out ₁ stl	00000010	rrrrrrrb	
7FC7	OUT _{1BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FC8	OUT _{2CS}	Control & Status	*	*	*	*	*	*	out ₂ bsy	out ₂ stl	00000010	rrrrrrrb	
7FC9	OUT _{2BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FCA	OUT _{3CS}	Control & Status	*	*	*	*	*	*	out ₃ bsy	out ₃ stl	00000010	rrrrrrrb	
7FCB	OUT _{3BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FCC	OUT _{4CS}	Control & Status	*	*	*	*	*	*	out ₄ bsy	out ₄ stl	00000010	rrrrrrrb	
7FCD	OU ₄ TBC	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FCE	OUT _{5CS}	Control & Status	*	*	*	*	*	*	out ₅ bsy	out ₅ stl	00000010	rrrrrrrb	
7FCF	OUT _{5BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FD0	OUT _{6CS}	Control & Status	*	*	*	*	*	*	out ₆ bsy	out ₆ stl	00000010	rrrrrrrb	
7FD1	OUT _{6BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	
7FD2	OUT _{7CS}	Control & Status	*	*	*	*	*	*	out ₇ bsy	out ₇ stl	00000010	rrrrrrrb	
7FD3	OUT _{7BC}	Byte Count	*	d ₆	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	xxxxxxxx	RW	

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	CPU	Notes
	Global USB Registers											Access	
7FD4	SUDPTRH	Setup Data Ptr H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW	
7FD5	SUDPTL	Setup Data Ptr L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW	
7FD6	USBCS	USB Control & Status	WakeSRC	*	*	*	DisCon	DiscOE	ReNum	SIGRSUME	00000100	brrrrbbb	Clear b7 by writing "1"
7FD7	TOGCTL	Toggle Control	Q	S	R	IO	0	EP2	EP1	EP0	xxxxxxxx	rbbbbbbb	
7FD8	USBFRAMEL	Frame Number L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R	
7FD9	USBFRAMEH	Frame Number H	0	0	0	0	0	FC10	FC9	FC8	xxxxxxxx	R	
7FDA		(reserved)											
7FDB	FNADDR	Function Address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	xxxxxxxx	R	
7FDC		(reserved)											
7FDD	USBPAAIR	Endpoint Control	ISOsend0	*	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN	0x000000	RW	PRx = 1 to pair EP
7FDE	IN07VAL	Input Endpoint 0-7 valid	IN7VAL	IN6VAL	IN5VAL	IN4VAL	IN3VAL	IN2VAL	IN1VAL	1	01010111	RW	VAL =1 means valid
7FDF	OUT07VAL	Output Endpoint 0-7 valid	OUT7VAL	OUT6VAL	OUT5VAL	OUT4VAL	OUT3VAL	OUT2VAL	OUT1VAL	1	01010101	RW	VAL =1 means valid
7FE0	INISOVAL	Input EP 8-15 valid	IN15VAL	IN14VAL	IN13VAL	IN12VAL	IN11VAL	IN10VAL	IN9VAL	IN8VAL	00000111	RW	VAL =1 means valid
7FE1	OUTISOVAL	Output EP 8-15 valid	OUT15VAL	OUT14VAL	OUT13VAL	OUT12VAL	OUT11VAL	OUT10VAL	OUT9VAL	OUT8VAL	00000111	RW	VAL =1 means valid
7FE2	FASTXFR	Fast Transfer Mode	FISO	FBLK	RPOL	RMOD1	RMOD0	WPOL	WMOD1	WMOD0	xxxxxxxx	RW	
7FE3	AUTOPTRH	Auto-Pointer H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW	
7FE4	AUTOPTL	Auto-Pointer L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW	
7FE5	AUTODATA	Auto Pointer Data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
7FE6		(reserved)											
7FE7		(reserved)											
	Setup Data												
7FE8	SETUPDAT	8 bytes of SETUP data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	R	
	Isochronous FIFO Sizes												
7FF0	OUT8ADDR	Endpt 8 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF1	OUT9ADDR	Endpt 9 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF2	OUT10ADDR	Endpt 10 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF3	OUT11ADDR	Endpt 11 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF4	OUT12ADDR	Endpt 12 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF5	OUT13ADDR	Endpt 13 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF6	OUT14ADDR	Endpt 14 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF7	OUT15ADDR	Endpt 15 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF8	IN8ADDR	Endpt 8 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FF9	IN9ADDR	Endpt 9 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFA	IN19ADDR	Endpt 10 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFB	IN11ADDR	Endpt 11 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFC	IN12ADDR	Endpt 12 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFD	IN13ADDR	Endpt 13 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFE	IN14ADDR	Endpt 14 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	
7FFF	IN15ADDR	Endpt 15 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0	xxxxxxxx	RW	